

Fig. 1a

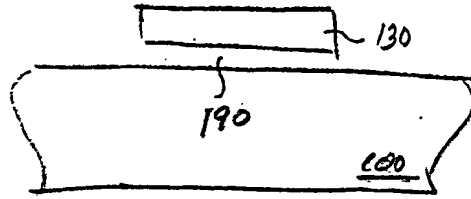


Fig. 1b

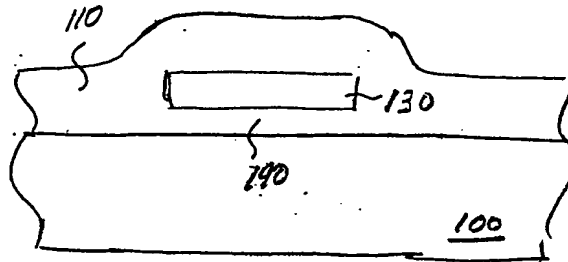


Fig. 1c

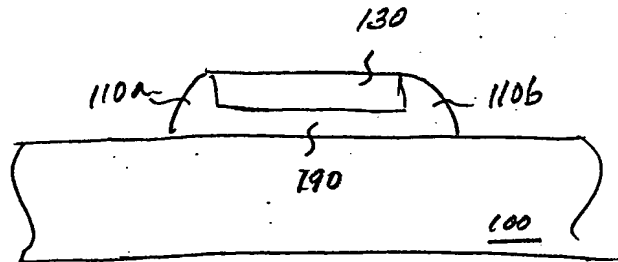


Fig. 1d

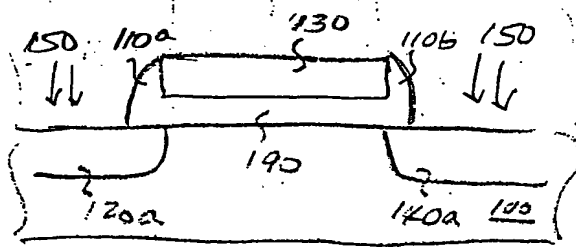


Fig. 1e

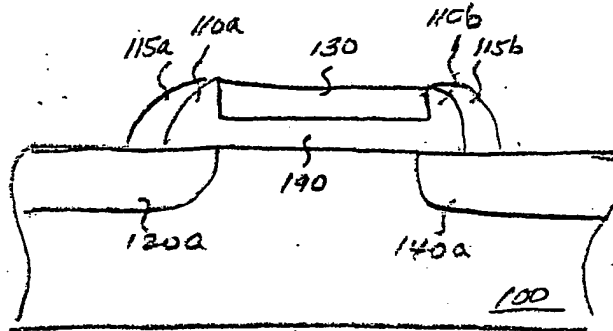


Fig. 1f

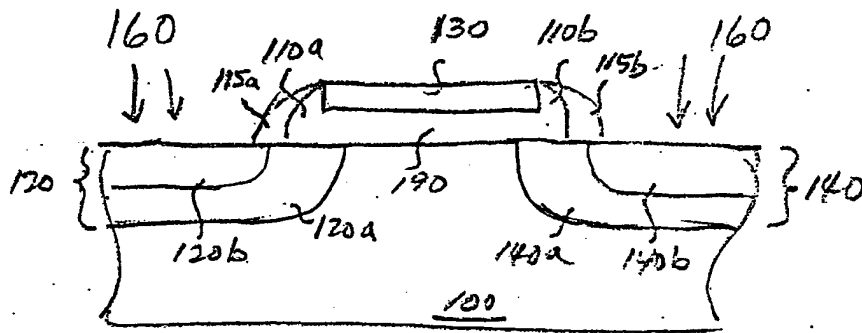
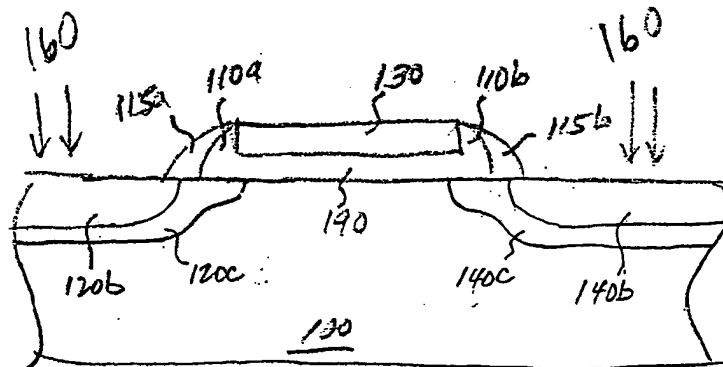
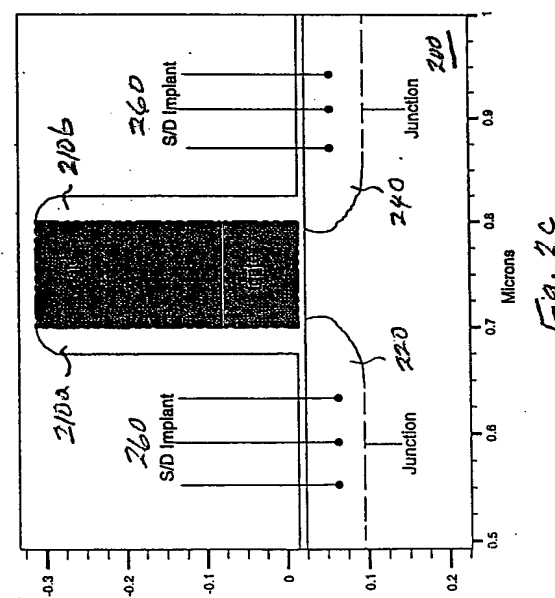
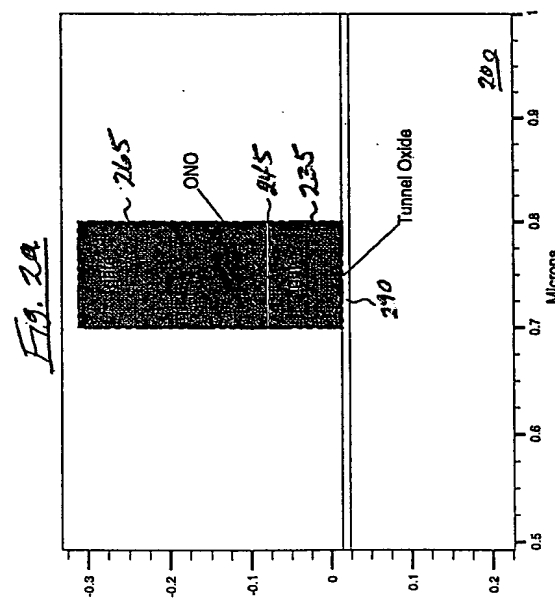
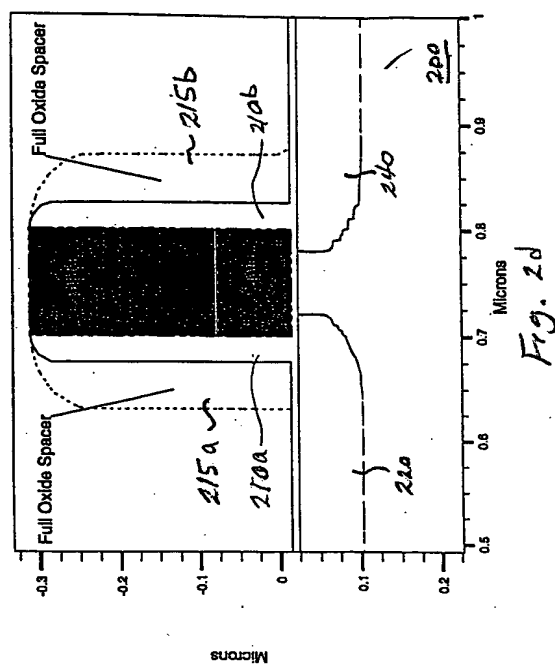
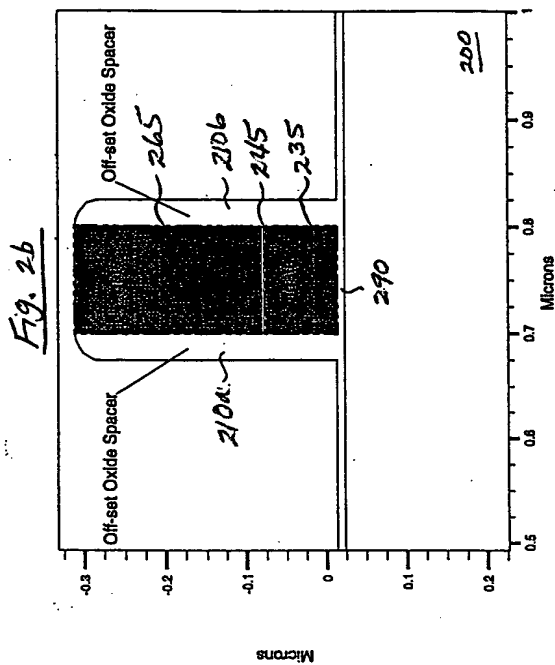


Fig. 1g



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Array Cell

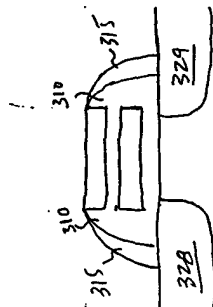
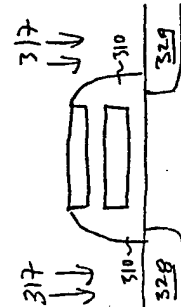
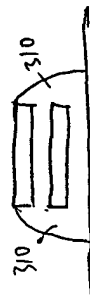
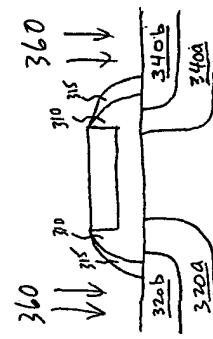
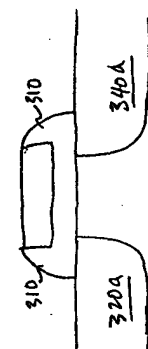
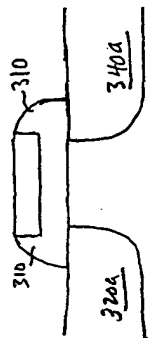
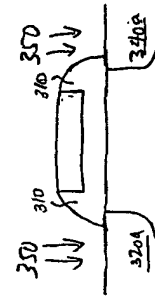
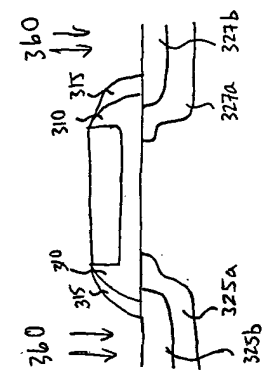
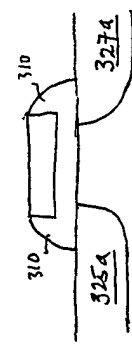
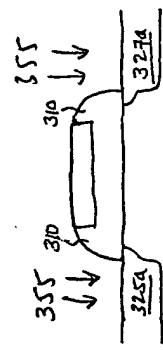
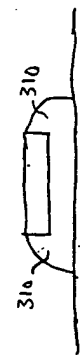


Fig. 3a



Brigdeny DDD
HV transistor



Periphery LDD

Fig. 4a

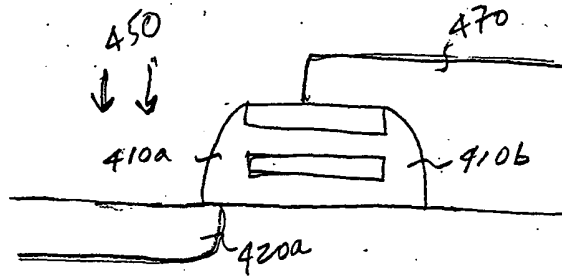


Fig. 4b

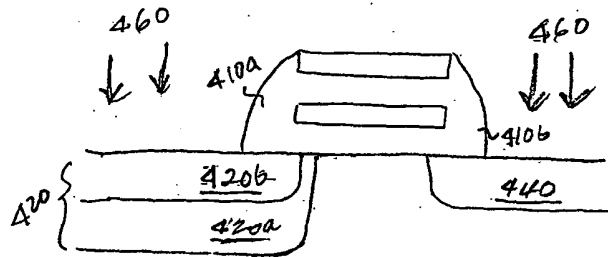


Fig. 5a

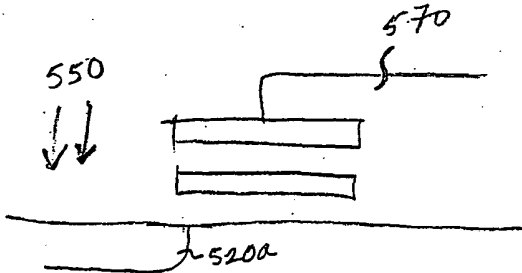


Fig. 5b

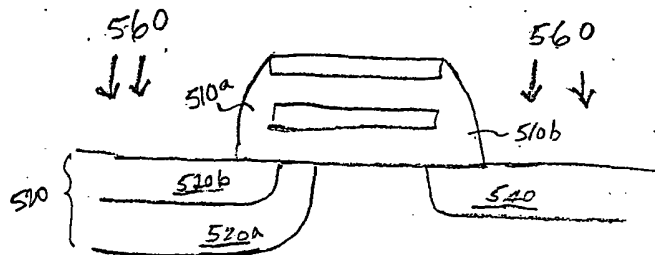


Fig. 6

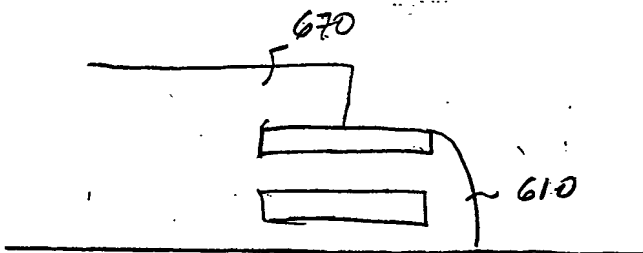


Fig. 7

